

1 Today, another higher bandwidth TDM system is in use. This
2 system is referred to as the synchronous optical network (SONET)
3 or, in Europe, the synchronous digital hierarchy (SDH). The SONET
4 network is designed to provide enormous bandwidth. SONET signals
5 are referred to as Synchronous Transport Signals (STS) or Optical
6 Carriers (OC). The narrowest SONET signal is referred to as STS-1
7 or OC-1. It has a bandwidth of 51.84 Mb/s which is sufficient to
8 carry twenty-eight DS1 signals or a single DS3 signal. The
9 hierarchy includes STS-3 (OC-3) which is three times the bandwidth
10 of an STS-1 (OC-1) signal, and higher bandwidth signals increasing
11 in multiples of four, i.e. STS-12 (OC-12), STS-48 (OC-48), STS-192
12 (OC-192), and STS-768 (OC-768).

14 SONET signals are said to be synchronous because all nodes in
15 the SONET network are synchronized to a common reference clock.
16 The older T-1 and T-3 signals are said to be plesiochronous
17 (nearly synchronous) because the clock rate of each signal is
18 tightly controlled. As used herein, however, all signals other
19 than SONET signals are referred to as asynchronous. When multiple
20 T-1 or T-3 signals from different sources are demultiplexed from a
21 SONET signal, each of these plesiochronous signals will have its
22 own separate clock. The clock for each signal is derived from the
23 SONET signal using a desynchronizer. For example, when
24 demultiplexing an STS-1 signal which carries twenty-eight DS-1
25 data signals, twenty-eight desynchronizers will be used to create

1 twenty-eight separate clock signals, one for each DS-1 signal. In
2 fact, each DS-1 signal will have its own clock, data, and frame
3 signals.

4
5 As telecommunication networks grow, it is desirable to
6 miniaturize network equipment as much as possible, particularly in
7 urban areas where space is expensive and networks are large. For
8 example, a SONET demultiplexer may be made of a few integrated
9 circuit chips. One of the difficulties in miniaturization is that
10 as more devices are placed on a single chip, more leads or pins
11 are required. The physical size of the chip limits the number of
12 leads which can be used. For example, in a SONET demultiplexer,
13 it would be necessary to provide three pins (clock, data, and
14 frame) for each "possible" asynchronous signal. By "possible", it
15 is meant that in a higher order SONET signal, such as an STS-3,
16 demultiplexing may involve separating out twenty-eight DS-1
17 signals and two STS-1 signals or it could involve separating out
18 up to eighty-four DS-1 signals. Thus, a demultiplexing solution
19 for an STS-3 would require eighty-four data lines, eight-four
20 clock lines, and eight-four frame signal lines in order to
21 terminate eighty-four DS-1 signals. This would require many
22 separate pins on a chip.

SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide methods and apparatus for simultaneously transferring synchronous and asynchronous signals among broadband access devices.

It is also an object of the invention to provide methods and apparatus for efficiently transferring synchronous and asynchronous signals among broadband access devices.

It is another object of the invention to provide methods and apparatus for transferring synchronous and asynchronous signals among broadband access devices using a minimum number of lines.

In accord with these objects which will be discussed in detail below, the apparatus of present invention provides a bus which includes a data bus, a clock bus, and a plurality of control lines which are used to indicate the type of data being carried on the data bus. According to the methods of the invention, data is transferred on the bus in a repeating frame having a plurality of slots, each slot being defined as one bus clock cycle. Each slot may contain a synchronous or asynchronous data signal and one or more of the control lines are asserted during the slot time of the data to indicate the type of data.

1 Two embodiments are provided. One utilizes a 25 MHz clock
2 bus and a repeating frame of three hundred thirty-six slots. The
3 other utilizes a 75 MHz clock bus and a repeating frame of one
4 thousand eight slots. In the first embodiment, data is
5 interleaved in groups of four and in the second embodiment data is
6 interleaved in groups of twelve. The first embodiment supports up
7 to four STS-1 payloads or combinations of other signals totalling
8 the same bandwidth. The second embodiment supports up to twelve
9 STS-1 signals or combinations of other signals totalling the same
10 bandwidth.

11
12 The presently preferred embodiment of the data bus includes
13 eight receive bits and eight transmit bits. The control lines
14 include RxIFSlot, TxIFSlot, RxValid, TxValid, RxFrm_ind,
15 TxFrm_ind, RxFrm_pos2-0, TxFrm_pos2-0, RxPrty, TxPrty2, and
16 TxPrty1. RxIFSlot (for the receive bus) and TxIFSlot (for the
17 transmit bus) are used to mark the first bus slot. They are
18 asserted low once every three hundred thirty-six time slots (one
19 thousand eight for the second embodiment). RxValid indicates the
20 presence of a valid data byte on the receive bus when it is
21 asserted low. TxValid indicates that the data byte on the
22 transmit bus is requested when it is asserted low. RxFrm_ind and
23 TxFrm_ind indicate the start of frame (not to be confused with the
24 repeating frame of the invention) of an asynchronous signal such
25 as a T-1, etc. RxFrm_pos2-0 and TxFrm_pos2-0 indicate the frame

1 pulse position within a byte when RxFrm_ind, respectively
2 TxFrm_ind, is asserted. A value of 111 indicates the MSB and 000
3 indicates the LSB. RxPrty, TxPrty2, and TxPrty1 are parity bits
4 which provide even parity over all (or some, depending on mode of
5 operation) the other control and data signals.

6
7 The invention is implemented in conjunction with an optical
8 network interface which is designated the sender and an interface
9 to another network, e.g. an interface to a router, which is
10 designated a receiver. The bus system according to the invention
11 is operable with multiple senders and receivers. It is therefore
12 applicable to an add/drop node of the optical network as well as
13 to an end point node.

14
15 Additional objects and advantages of the invention, including
16 the details of multiplexing synchronous and asynchronous signals
17 in both the first and second embodiment will become apparent to
18 those skilled in the art upon reference to the detailed
19 description taken in conjunction with the provided Appendix.

20 21 BRIEF DESCRIPTION OF THE DRAWINGS

22
23 Figure 1 is a simplified block diagram of a simple embodiment
24 of the apparatus according to the invention showing two devices
25 coupled to a bus;

1 Figure 2 is a diagram of the repeating frame of a first
2 embodiment of the invention; and
3

4 Figure 3 is a block diagram similar to Figure 1 but showing
5 four devices coupled to the bus.
6

7 BRIEF DESCRIPTION OF THE APPENDIX 8

9 The attached sixty-six page Appendix is a document entitled
10 Extendible Asynchronous and Synchronous Interface (EASI) Bus for
11 Broadband Access - Functional Requirements which includes numerous
12 figures, tables and timing diagrams illustrating operation of the
13 invention.
14

15 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS 16

17 Turning now to Figure 1, the apparatus of present invention
18 provides a bus 10 which includes a receive (Rx) data bus 11, a
19 transmit (Tx) data bus 12, a clock bus 14, and a plurality of
20 control lines 15 which are used to indicate the type of data being
21 carried on the Rx and Tx data buses. The presently preferred
22 embodiment of the Rx bus 11 includes eight receive bits and the Tx
23 bus 12 eight transmit bits. The control lines include RxIFSlot,
24 TxIFSlot, RxValid, TxValid, RxFrm_ind, TxFrm_ind, RxFrm_pos2-0,
25 TxFrm_pos2-0, RxPrty, TxPrty2, and TxPrty1. As shown in Figure 1,

1 a first device (bus user) 16 is coupled to a second device (bus
2 user) 18 via the bus 10; i.e. the data buses 11, 12, the clock bus
3 14, and the control lines 15. The clock bus 14 is coupled to a
4 clock source 20.

5
6 According to the invention, the first device 16 is coupled
7 via a standard SONET interface (not shown) to an optical network
8 22 and is considered to be a "Sender". The second device 18 is
9 coupled to a non-SONET network 24 via an ETHERNET or other non-
10 SONET interface (not shown) and is considered to be a "Receiver".
11 Details concerning the Sender are set out in the attached Appendix
12 at pages 28-38 and 55-62. Details concerning the Receiver are set
13 out in the Appendix at pages 19-28 and 50-55.

14
15 As used herein, the terms Sender and Receiver are not the
16 same as the terms Master and Slave which are often used to
17 describe devices coupled to a bus. According to the invention,
18 either the Sender or the Receiver can act as bus Master. Appendix
19 pages 50-62 include timing diagrams illustrating the Sender and
20 Receiver operating in both Master Mode and Slave Mode.

21
22 Before discussing the operation of the apparatus and in
23 particular, the operation of the control lines, it is useful to
24 first understand the repeating frame by which data is transferred
25 over the bus.

1 Turning now to Figure 2, according to a first embodiment of
2 the invention which operates at a bus speed of 25 MHz, the frame
3 has three hundred thirty-six time slots. Data is interleaved in
4 groups of four slots which corresponds to the STS-1 slot
5 interleave scheme. The first embodiment supports the transfer
6 from the optical network 22 to the non-optical network 24 (or vice
7 versa) up to four STS-1 payloads or combinations of other signals
8 totalling the same bandwidth. Examples of the types of signals
9 which can be mapped into the frame are illustrated in the attached
10 Appendix at pages 7-14.

11
12 A second embodiment of the invention is shown in the attached
13 Appendix at pages 40-49. The second embodiment operates at a bus
14 speed of 75 MHz and uses a repeating frame of one thousand eight
15 slots. In the second embodiment data is interleaved in groups of
16 twelve. The second embodiment supports the transfer of up to
17 twelve STS-1 signals or combinations of other signals totalling
18 the same bandwidth. Examples of the types of signals which can be
19 mapped into the frame of the second embodiment are illustrated in
20 the attached Appendix at pages 44-49.

21
22 Referring now to Figures 1 and 2, the signals RxIFSlot (for
23 the receive bus) and TxIFSlot (for the transmit bus) are used to
24 mark the first slot in the frame. They are asserted low once

1 every three hundred thirty-six slots for the first embodiment and
2 once every one thousand eight slots for the second embodiment.

3
4 RxValid indicates the presence of a valid data byte on the
5 receive bus when it is asserted low.

6
7 TxValid indicates that the data byte on the transmit bus is
8 requested (or that it is being sent depending on the mode of
9 operation) when it is asserted low.

10
11 The RxValid and TxValid signals are used to indicate when no
12 data is available in an asynchronous signal.

13
14 RxFrm_ind and TxFrm_ind indicate the start of frame (not to
15 be confused with the repeating frame of the invention) of an
16 asynchronous signal such as a T-1, E-1 etc.

17
18 RxFrm_pos2-0 and TxFrm_pos2-0 indicate the frame pulse
19 position within a byte when RxFrm_ind, respectively TxFrm_ind is
20 asserted. A value of 111 indicates the MSB and 000 indicates the
21 LSB.

22
23 RxPrty, TxPrty2, and TxPrty1 are parity bits which provide
24 even parity over all (or some, depending on mode of operation) the

1 other control and data signals. Details regarding the parity bits
2 can be found in the attached Appendix at pages 29 and 30.

3
4 Timing diagrams illustrating the operation of the Receiver in
5 both master and slave mode are shown at pages 22 and 50 of the
6 Appendix. Timing diagrams illustrating operation of the Receiver
7 in slave mode are shown at pages 23 and 52 of the Appendix.
8 Timing diagrams illustrating operation of the Receiver in master
9 mode are shown at pages 25, 26 and 54 of the Appendix.

10
11 A timing diagram illustrating operation of the Sender in both
12 master mode and slave mode is shown at page 56 of the Appendix.
13 Timing diagrams illustrating operation of the Sender in master
14 mode are shown at pages 32, 34, 35, 36, and 58 of the Appendix.
15 Timing diagrams illustrating operations of the Sender in slave
16 mode are shown at pages 37, 38, and 60 of the Appendix.

17
18 The bus of the invention is extensible. Figure 3 illustrates
19 a bus 110 coupled to two senders 116, 117 and two receivers 118,
20 119. In this example, the sender 116 operates in master mode and
21 all of the other devices operate in slave mode.

22
23 There have been described and illustrated herein several
24 embodiments of an extendible asynchronous and synchronous
25 interface bus for broadband access. While particular embodiments

1 of the invention have been described, it is not intended that the
2 invention be limited thereto, as it is intended that the invention
3 be as broad in scope as the art will allow and that the
4 specification be read likewise. Thus, while particular
5 combinations of synchronous and asynchronous signals have been
6 shown in the Appendix, it will be appreciated that other
7 combinations could be utilized. Also, while the bus has been
8 illustrated with one sender with one receiver, one sender with two
9 receivers, and two senders with two receivers, it will be
10 recognized that other combinations of senders and receivers could
11 be used. It will therefore be appreciated by those skilled in the
12 art that yet other modifications could be made to the provided
13 invention without deviating from its spirit and scope as so
14 claimed.